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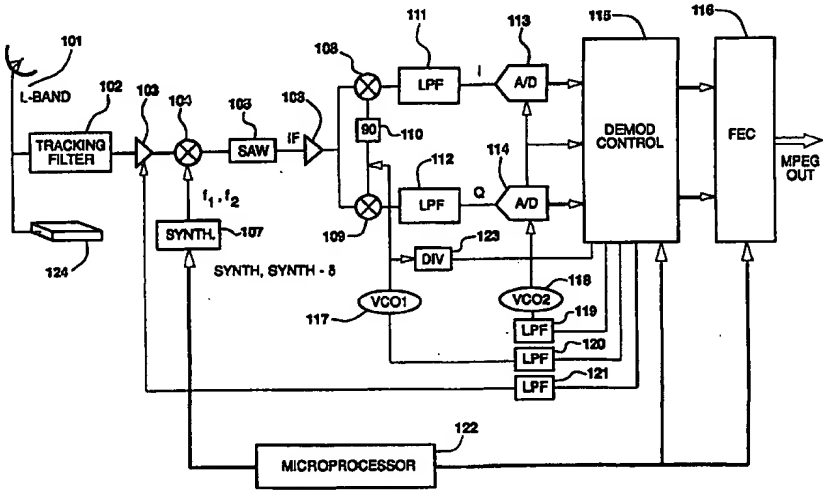

(57) Abstract

The present invention relates to an improved demodulator for locking onto and tracking a carrier. Harmonic frequencies are occasionally generated by demodulation circuitry. When this occurs, the harmonic frequencies can interfere with the demodulator's locking and tracking functions, especially if the harmonic frequencies are near a down converted carrier's frequency. A system and method are disclosed which provide an offset to a frequency synthesizer whose output frequency is used to down convert the carrier. The offset alters the frequency of the down converted carrier so as to shift it away from the interfering harmonics. In this regard, the demodulator is enabled to lock onto and track a carrier when previously not possible.

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SYSTEM AND METHOD FOR HARMONIC INTERFERENCE AVOIDANCE IN CARRIER RECOVERY FOR DIGITAL DEMODULATION

BACKGROUND OF INVENTION

1. Technical Field

This invention described herein relates generally to the demodulation of digital signals. More particularly, the invention described herein relates to controlling a down conversion frequency to account for harmonics resident in a demodulator.

2. Related Art

Demodulation is a widely used process to make very high frequencies usable. One of the carrier recovery techniques in digital demodulation is based on the presence of a VCO (Voltage Controlled Oscillator) in the recovery loop. The VCO performs two functions: first, it searches for the carrier frequency in a procedure called a "frequency sweep" and second it tracks the carrier once the recovery loop locks. This is important as the frequency offset that it tracks might be up to +/-5 MHz. This frequency drift is mostly caused by low noise amplifier drift (LNA).

In real systems, the problem of harmonics arises. Harmonics are generally additional spectral components which can interfere with a carrier recovery loop. In particular, a major problem is the chance that oscillator harmonics are present in the neighborhood of the VCO. If the harmonics fall within the capture/ tracking range of the carrier recovery loop, there is a chance that (due to coupling) the VCO will become disturbed and either fail to lock or break lock once acquired. Measurements show that this interference could cause from 1 to 5 dB loss. Specifically, this interference may be high enough in some cases to make the acquisition impossible (if the IF

carrier falls over the harmonic) or to desynchronize the demodulator or the FEC decoder (if tracking polls the VCO frequency over the harmonic) especially when operating in noisy channel.

This problem also occurs in carrier recovery loops that do not include super heterodyning processes. While increasing the operating tolerances by requiring more expensive components with regard to standard VCO processes may minimize the creation of the harmonics, it fails to accommodate for the existence of the harmonics in sensitive frequency bands. Accordingly, a solution is needed which accommodates real world harmonics while making the carrier recovery

SUMMARY OF THE INVENTION

The present invention overcomes the aforementioned problems as it accommodates for harmonics in various frequency bands. The disclosed system is useful in satellite receiver and cable television receivers which require the recovery of a carrier signal.

The system and method disclosed herein solves the problems of interference by various harmonics by locking onto a down converted carrier, and if no lock, then by locking on to an offset version of the down converted carrier. Next, the system and method relocates the down converted carrier to a new location on the swept frequency band, far away from the harmonic and other degrading frequencies (for example, the roll off frequency of a SAW filter). By employing the disclosed invention, a demodulator will function properly even in the presence of degrading harmonics.

BRIEF DESCRIPTION OF THE DRAWINGS

The present invention will now be described in more detail with reference to preferred embodiments of the invention, given only by way of example, and illustrated in the accompanying drawings in which:

Figure 1 shows a first hardware environment of the present invention;

Figure 2 shows the voltage signal applied to an oscillator of a carrier recovery loop as contemplated by embodiments of the present invention.

Figure 3 shows the carrier recovery loop locking onto a carrier signal a contemplated by embodiments of the present invention.

Figure 4 shows a flowchart as contemplated by embodiments of the present invention.

Figures 5 and 6 show signal diagrams as contemplated by embodiments of the present invention.

DETAILED DESCRIPTION

The present invention is discussed below with reference to the recovery of digital signals. It understood that the invention is readily applied to the recovery of other non-digital signals as well.

Figure 1 shows a block diagram of different components as contemplated by the present invention. An L-band digital signal 101 is received from a digital source (for example, a satellite receiver) and tracked by a tracking filter 102. Also, additional inputs of digital source include digital cable distribution systems. Also, in alternative embodiments, non-digital inputs are received as well including from analog television systems as well as from radio transmission systems. These systems are only given as examples. The application of the invention described herein is contemplated for a variety of uses where harmonic signals exists and need to be accommodated.

The output of the tracking filter 102 is fed through controlled amplifier 103. Controlled amplifier is controlled by demodulation control 115 for automatic gain control purposes. The output of controlled amplifier is fed into mixer 104 where it is down converted into an

intermediate frequency (IF). Mixer 104 uses a signal output from synthesizer 107. As shown in Figure 1, the output of synthesizer 107 is controlled to be a set frequency. Here, synthesizer 107 is controlled to output a signal at a first frequency and, upon control from microprocessor 122, output the signal at a second frequency. For simplicity, the two frequencies are referred to as f(synth) and f(synth-delta) where delta is an offset which changes the output of synthesizer 107. To control synthesizer 107, microprocessor 122 outputs one of at least two signals of SYNTH, and SYNTH-DELTA.

Next, the output from mixer 104 is passed through standing acoustical wave (SAW) filter 105 where the IF signal is filtered to remove unwanted characteristics. Finally, IF signal is passed through amplifier 106 and then to a baseband processing system.

Baseband processing system contains a number of different sub-circuits. The output from amplifier 106 is split into two paths I and Q, where I represents the in-phase component of the IF signal and Q represents the quadrature component of the IF signal. Referring first to the I path, IF signal is mixed at mixer 108 with a 90 degrees shifted output from voltage controlled oscillator 117 (VCO1). The phase shift is accomplished by phase shifter 110. The output from mixer 108 is passed through low pass filter (LPF) 111, through A/D converter 113, then to demodulation control 115. The path of Q is similar to that of I, using mixer 109, LPF 112, and A/D converter 114. The output of demodulation control 115 is fed into forward error correction circuit 116 and output as a desired signal. For example, the desired signal output is contemplated to be an MPEG output signal.

Once the system locks onto the carrier frequency $F_{lock\text{-}int}$, demodulation controller 115 evaluates the frequency $F_{lock\text{-}int}$ using the pre-scaled signal from VCO1 through DIV 123 to determine how close the VCO1 frequency is from the harmonic.

Next, the microprocessor changes the frequency of the synthesizer 107 with the offset value which will cause carrier recovery lock at a frequency between the harmonic and the limit where the filtering (SAW or baseband) starts degrading the spectrum of the signal.

The sweep signal is enabled thereafter but with a much smaller amplitude as the system knows approximately where the frequency $F_{final\text{-}lock}$ is. In particular, the narrow sweep only has to be wider than the synthesizer step. In this way, the acquisition at the new frequency $F_{lock\text{-}final}$ is done much faster then the initial one at $F_{lock\text{-}int}$.

Demodulation control 115 outputs a variety of control signals. First, it outputs an automatic gain control signal, passed through LPF 121, which controls amplifier 103, discussed above. Second, demodulation control 115 outputs a carrier recovery loop signal, passed through LPF 120, for VCO1 117. Finally, demodulation control 115 outputs symbol clock recovery signal, passed through LPF 119, for VCO2 118 so as to enable A/D converters 113 and 114 to know when each symbol to be decoded starts. To assist in the symbol clock recovery loop, the demodulation controller uses divider DIV 123 to scale down the frequency from VCO1 117 to determine what the clock recovery frequency out to VCO2 118 should be.

In this example, the most prevalent harmonic arises from this loop including VCO2 118. It is this harmonic for which the present invention accounts. However, other harmonics exist as well and are, likewise, avoided. Further, harmonics may arise from external locations (for example, from a timing circuit in another microprocessor). Embodiments of the present invention further contemplate avoiding these additional harmonics as well.

In addition to controlling synthesizer 107, microprocessor 122 also controls demodulation control 115 and forward error correction 116.

Turning attention to the carrier recovery loop including VCO1, the carrier recovery

circuitry performs two main functions: it searches for a down-converted carrier frequency through a procedure referred to as "frequency sweep" and it tracks the carrier once the recovery loop locks. As to the tracking function, the carrier recovery circuitry is enabled to track frequency drifts up to +/- 5 MHz. These drifts are mostly caused by low noise amplifier (LNA) drift.

Figure 2 shows the voltage output signal to VCO1 117 as contemplated by embodiments of the present invention. Figure 2 shows two sets of frequency sweeps. The first is referred to the period of f(synth). This period includes two equal time intervals t_1 and a time interval t_2. These two time intervals show the voltage output from VCO1 117 as having two slopes m_1 (and $-m_1$) and m_2. During application of the offset frequency period f(synth-delta) and as the offset frequency is set so as to include the carrier frequency, the length of the internal time periods t_3 and t_4 are adjusted to be much shorter. In this example, embodiments of the present invention contemplate the slopes m_1 and m_2 of the voltage waveform input into VCO1 117 as remaining the same values. The sweep signal as shown in Figure 2 has the two different slopes m_1 and m_2 so the resulting sweep is slow enough (m_2) to lock on the carrier signal at the worst signal to noise ratio (SNR) that the system is specified to work. At high SNR, however, the sweep (m_1) is allowed to be relatively fast in order to minimize the acquisition time of the carrier.

Embodiments of the present invention contemplate the voltage provided by the demodulation controller to the VCO1 117 as ideally linear. Alternatively, non-linear sweeps are envisioned as well as to allow for precise control over the sweeping interval. The peak to peak value of the signal of Figure 2 determines the frequency swing around the expected IF carrier (as generally represented at 480 MHz for terrestrial applications or 70 MHz in satellite receivers).

As shown in Figure 2, the f(synth) period is followed by the f(synth-delta) period. The alteration of one waveform then the other wave form allows for fast acquisition of the down

converted carrier signal as, if the carrier is not acquired during the f(synth) period, then altering the down conversion carrier frequency may likely acquire the carrier during the f(synth-delta) period. Alternatively, the present invention contemplates sweeping with the f(synth) period multiple times before switching to the f(synth-delta) period. This method allows for system averaging accounting for transient reception effects (for example, temporary blockage of the carrier signal). Moreover, the present invention contemplates a third scheme for initiating the f(synth-delta) period where the f(synth-delta) is only initiated after an established lock and subsequent failure (for example, when the carrier frequency shifts due to LNA).

Figure 3 shows the output of VCO1 117 during the harmonic avoidance scheme. $F_{saw(min)}$ and $F_{saw(max)}$ represent the minimum and maximum frequencies allowed to pass through SAW filter 105. Accordingly, all down converted carriers frequencies should be controlled to fall within this range. Further, embodiments of the present invention contemplate keeping, for example, F_{min} apart from $F_{saw(min)}$ because of the relatively fast roll off of signal strength near the edges of the SAW filter's cut off frequencies. Using the sweep generated by the demodulation control, VCO1 117 sweeps through its controlled frequency range F_{min} to F_{max}. As shown here, the harmonic frequency $f_{harmonic}$ is close to the actual down converted carrier frequency $F_{lock-in}$. Accordingly, while the carrier recovery loop with VCO1 may, as shown here, or may not actually lock onto the down converted carrier signal, the closeness of the harmonic frequency to the carrier frequency may disrupt the operation of the carrier recovery loop. In the example of Figure 3, the carrier recovery loop looses lock at time t_d. When this occurs, or when the carrier recovery loop cannot lock onto the carrier frequency, the microprocessor (or micro controller) 122 alters the synthesizer's down converting frequency from F(synth) to F(synth-delta). In this regard, the carrier recovery loop starts sweeping for the carrier using shorter intervals at time t_d. At sweep

time t_j, the final lock is achieved onto the down converted carrier frequency.

Using this procedure, the carrier recovery loop will eventually lock and a true/ false lock decision is made by the controller or by the microprocessor. If the lock is not onto the proper carrier (for example, a false lock onto an alternate phase of the carrier), then the system breaks lock until the correct lock is achieved. Also, if too many errors are generated by the harmonic, through reducing the SNR beyond a threshold level, the system again breaks lock and repeats the acquisition process until a true lock has been achieved. The true/false lock determination is described in greater detail in U.S. Serial No. 08/427,660, entitled "Method And Apparatus For Locating And Tracking A QPSK Carrier" which is a continuation of U.S. Serial No. 08/160.839, entitled "Method And Apparatus For Locating And Tracking A QPSK Carrier", now abandoned, which is incorporated by reference for all necessary disclosure.

As shown in Figure 3, the forming and breaking of lock is shown as the frequency $F_{lock\text{-}int}$. The present invention contemplates that the frequency sweep range (from F_{min} to F_{max}) to be larger than the expected LNA offset plus the synthesizer resolution step and SAW filter. Also, embodiments of the present invention contemplate baseband LPF should not distort the spectrum of the signal. Also, for noise reduction purposes, embodiments of the present invention contemplate separating F_{min} and F_{max} from the cut off frequencies ($F_{saw(min)}$ and $F_{saw(max)}$) of the SAW filter because of signal degradation near these cut off frequencies. Therefore, the system offers enough clearance from the distortion at $F_{saw(min)}$ and $F_{saw(max)}$ so as to accommodate the sweep and the lock of the carrier recovery loop even at the extreme of the sweep cycle.

As noted in Figure 3, the shifted carrier frequency is adjusted so as to be as far away from degrading frequencies as possible. In this case, the carrier frequency is adjusted to be equally between the initial lock frequency (which failed previously to lock) $F_{lock\text{-}int}$ and one of the

frequencies of SAW filter $F_{saw(min)}$. For the example of Figure 3, $F_{saw(min)}$ is preferable to move to as the harmonic is closer to $F_{saw(max)}$ that $F_{saw(min)}$. In another example, the $F_{lock-final}$ frequency is moved in the direction of $F_{saw(max)}$ to avoid a harmonic closer to $F_{saw(min)}$. In yet another example as shown in Figure 4, the $F_{harmonic}$ frequency and at least one of the F_{min} and F_{max} frequencies are used to place the $F_{lock-final}$ frequency. It should be noted that the frequencies in which to avoid are those containing degrading characteristics. In the above examples, the frequency of F_{min} was chosen over the frequency $F_{saw(min)}$ in one example (and reversed in another example) as determining which set of frequencies to use is system specific as to avoid noisy frequencies. For instance, if $F_{saw(min)}$ was far from F_{min}, then present embodiments of the invention contemplate F_{min} as the lower frequency limit as moving too far in the direction of $F_{saw(min)}$ may extend $F_{final-lock}$ below F_{min}. The same process is readily applied to the upper frequencies as well.

It should be noted that the selection of the number of wide search bands and the number of narrow search bands as contemplated by embodiments of the present invention are shown here, by example, near a one to one correspondence. Embodiments of the present invention additionally contemplate multiple versions of each. For example, another example includes 4 wide searches to a single narrow search.

Figure 4 shows a flowchart as contemplated by embodiments of the present invention. In which two frequency shifting operations are performed. At step 401, the system determines whether a harmonic is present which may disrupt carrier recovery operations. If there is no carrier, the system (for example, an integrated receiver-decoder) locks onto the down converted carrier using regular procedures as shown above with respect to Figure 1, as shown by step 402. If there is a harmonic signal present, then the system determines (for example, through a sensing operation of microprocessor 122 or through manual input of internal clock frequencies) the

frequency of the harmonic (or harmonics, as the case may be). The system next attempts to lock the carrier recovery unit onto the carrier signal at step 404. To do this, the tuner is controlled to sweep in the wide fast/slow sweep using alternating frequency offsets. Here, the frequency offset is 250 kHz. Figure 5 shows the wide fast/slow sweep pattern centered about, for example 480 MHz. An example of the 250 kHz offset applied is shown in Figure 6 by the inclusion of delta$_f$ in one cycle. At this point, the carrier should be locked, albeit possibly near the harmonic frequency. Next, at step 405, the frequency of the VCO1 is read through divider 123.

The next portion of the carrier locking scheme as shown in Figure 4 relates to separating the carrier's down converted frequency from the harmonic frequency. As shown in step 406, the scheme determines if the harmonic frequency is above or below the down converted carrier frequency. Through the equations at steps 407 and 409 or through the equations at steps 408 and 410, the center frequency for the narrow sweep as shown through time periods t_d through t_j in Figure 3 is determined. It should be noted that, in this example, the frequency of the synthesizer is placed above that of the received signals. If, however, one desired to have the frequency of the synthesizer placed below that of the received signals, the equations used would be similar but with minor modifications as apparent to one of ordinary skill in the art.

Next, new frequency of the synthesizer 107 is determined as offset from the original frequency by f_{off} as shown in step 411. The scheme sweeps for a number of cycles as shown in step 412. Here, for example, the number of sweeps is 4. This number is adjusted to account for any transient signals which may occur so as to maximize the chances for a new lock at the newly adjusted carrier frequency. At step 413, the system determines whether the carrier recovery loop has locked. If yes, then as shown in step 414, the scheme determines if this is a proper lock, far from any problems (for example, locking on an out of phase false carrier or excessive error

signals). If this is a good lock as determined in step 415, then the scheme loops back to step 414 to continue to monitor the quality of the lock. If not a good lock, the scheme loops back to step 412 until the limit on the number of sweep cycles is reached. From step 413, if no lock is found, then the system changes back to the wide sweep back at the original carrier down converted frequency shown here, for example, as the sweep centered at 480 MHz with a +/- 3 MHz sweep.

It should be noted that if the LNA offset is more than expected, multiple filtering steps may be required to reduce the harmonic signal. Examples of where to place the filters include additional filtering on the SAW and base band signals.

While particular embodiments of the present invention have been described and illustrated, it should be understood that the invention is not limited thereto since modifications may be made by persons skilled in the art. The present application contemplates any and all modifications that fall within the spirit and scope of the underlying invention disclosed and claimed herein.

WHAT IS CLAIMED IS:

1. A demodulator including a recovery loop in which a harmonic signal at a harmonic frequency disrupts capture or tracking of a carrier signal comprising:

an input for receiving a carrier signal at a carrier frequency modulated with a data signal;

a frequency generator for generating a signal at a first frequency;

a converter for converting the carrier signal at the carrier frequency to a lower frequency in response to said signal from said frequency generator;

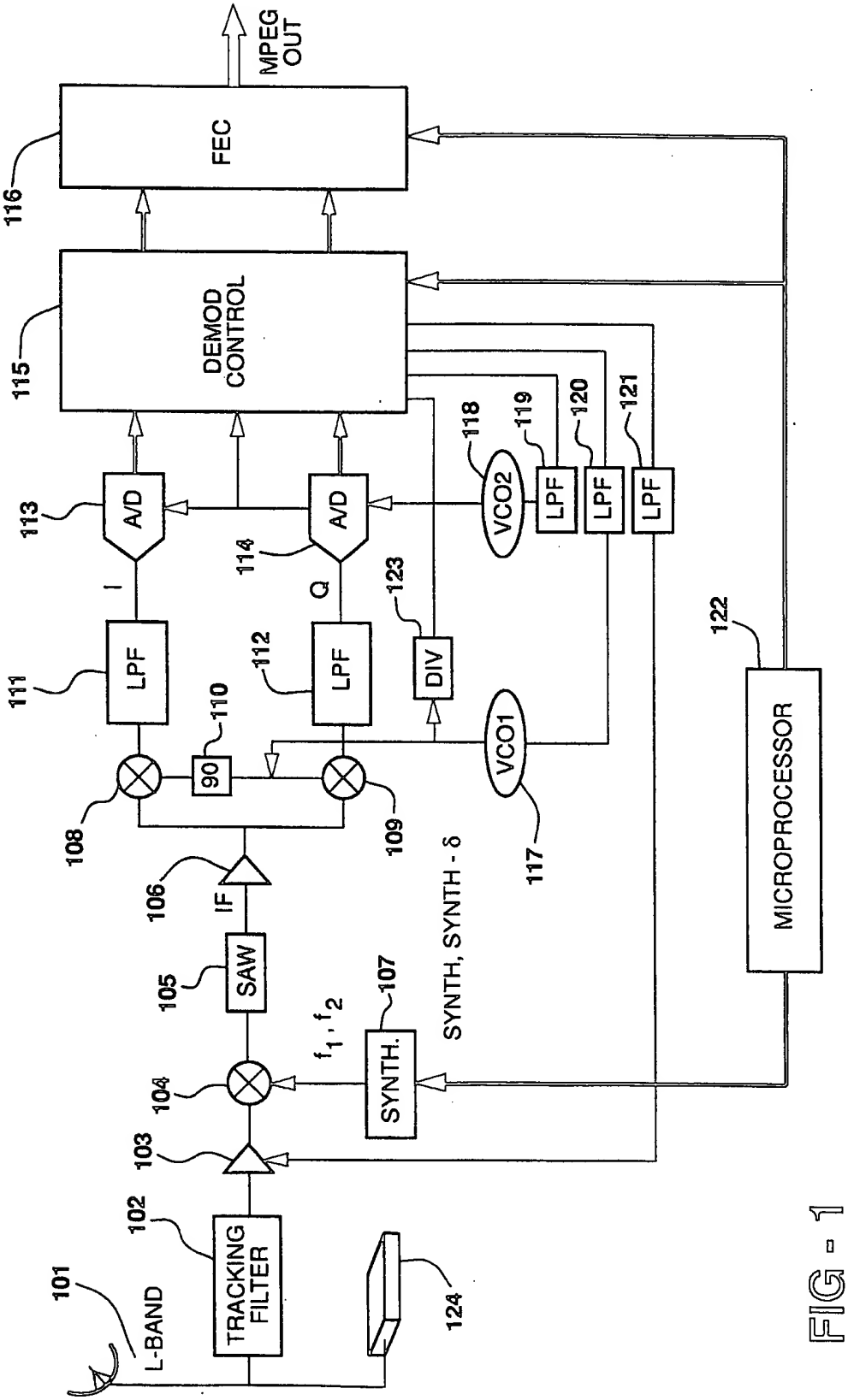
a controller for controlling said frequency generator;

a locking circuit for locking onto said lower frequency;

wherein said controller controls said frequency generator to generate said signal at a second frequency offset from said first frequency so that the lower frequency from said converter is further separated from the harmonic frequency.

2. The demodulator according to claim 1, wherein said controller determines how close the harmonic frequency is to said down converted carrier frequency.

3. The demodulator according to claim 1, wherein said locking circuit uses two different sweep times for locking onto said carrier.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LPF
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LPF
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LPF
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VCO1
117
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110
108
109
106
IF
SAW
105
104
103
SYNTH.
107
f_1, f_2
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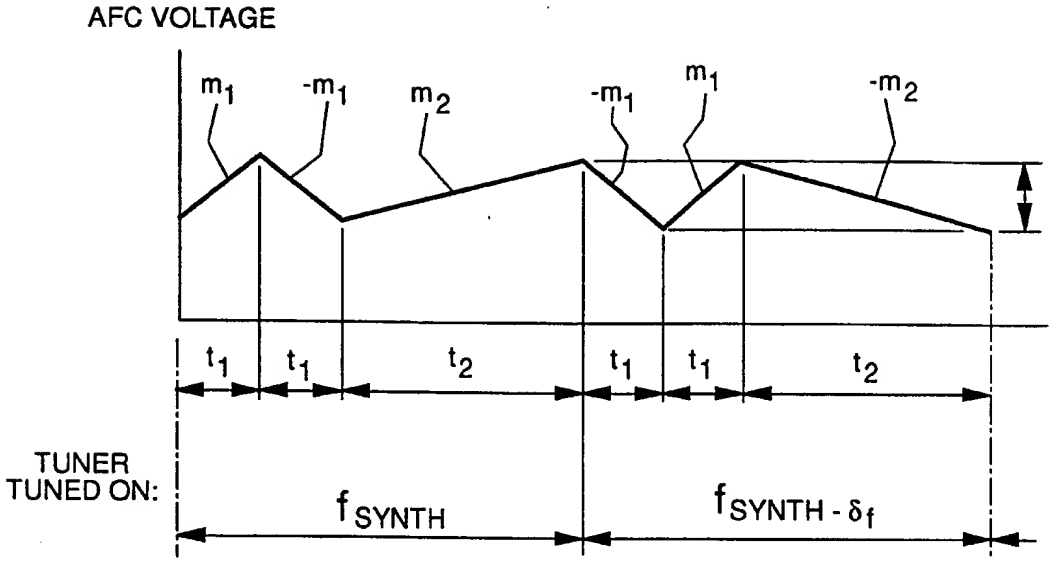
MICROPROCESSOR
122
TRACKING FILTER
102
L-BAND
101
124

FIG - 1

FIG - 2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m1
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fSYNTH
fSYNTH - δf

FIG - 5

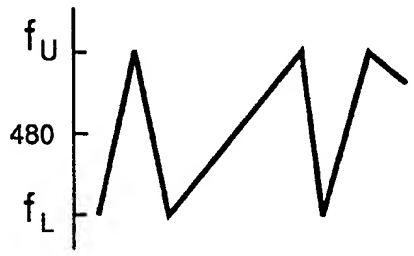
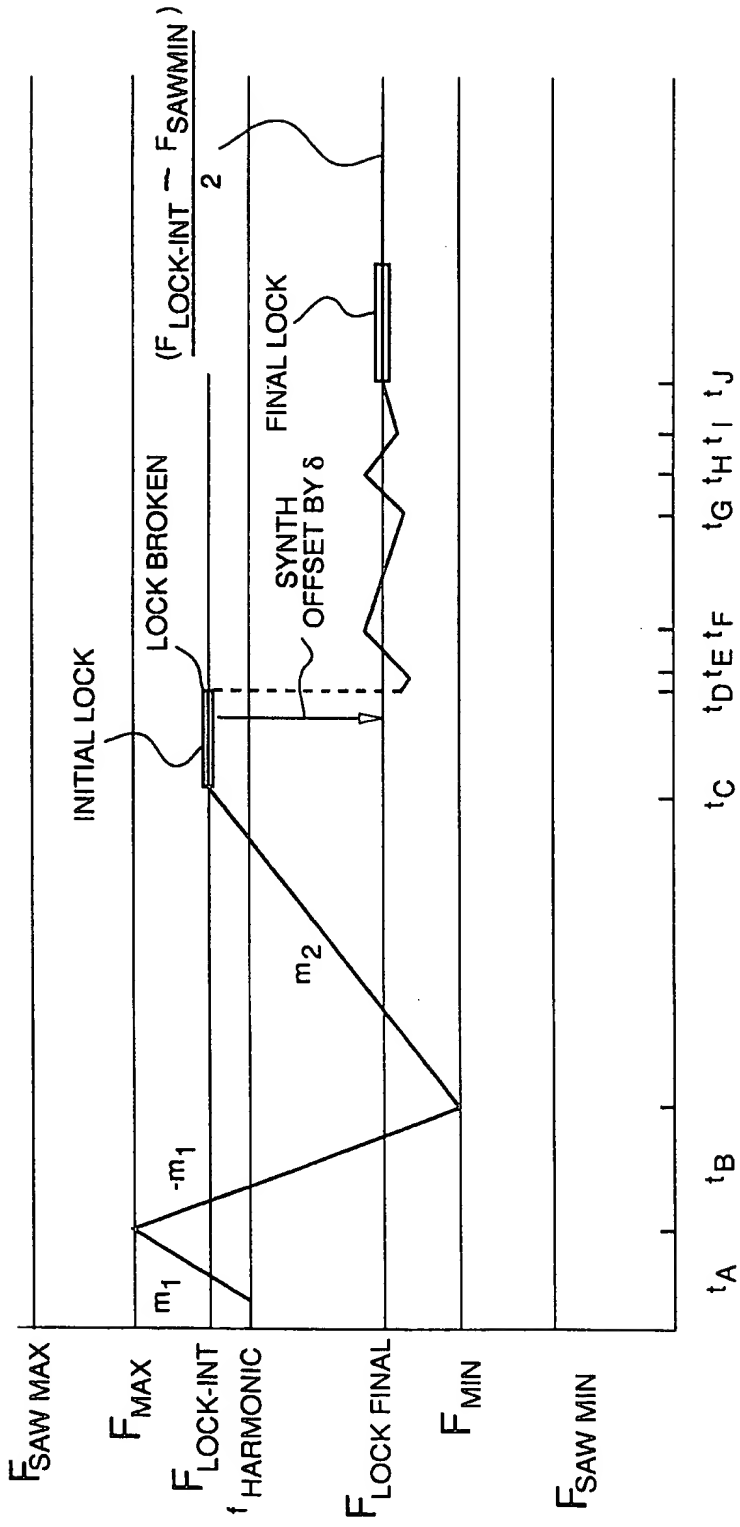

fU
480
fL

FIG - 3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$F_{LOCK\text{-}INT}$
$f_{HARMONIC}$
$F_{LOCK\ FINAL}$
F_{MIN}
$F_{SAW\ MIN}$
INITIAL LOCK
LOCK BROKEN
$(F_{LOCK\text{-}INT} \sim F_{SAWMIN})/2$
SYNTH OFFSET BY δ
FINAL LOCK
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m_2
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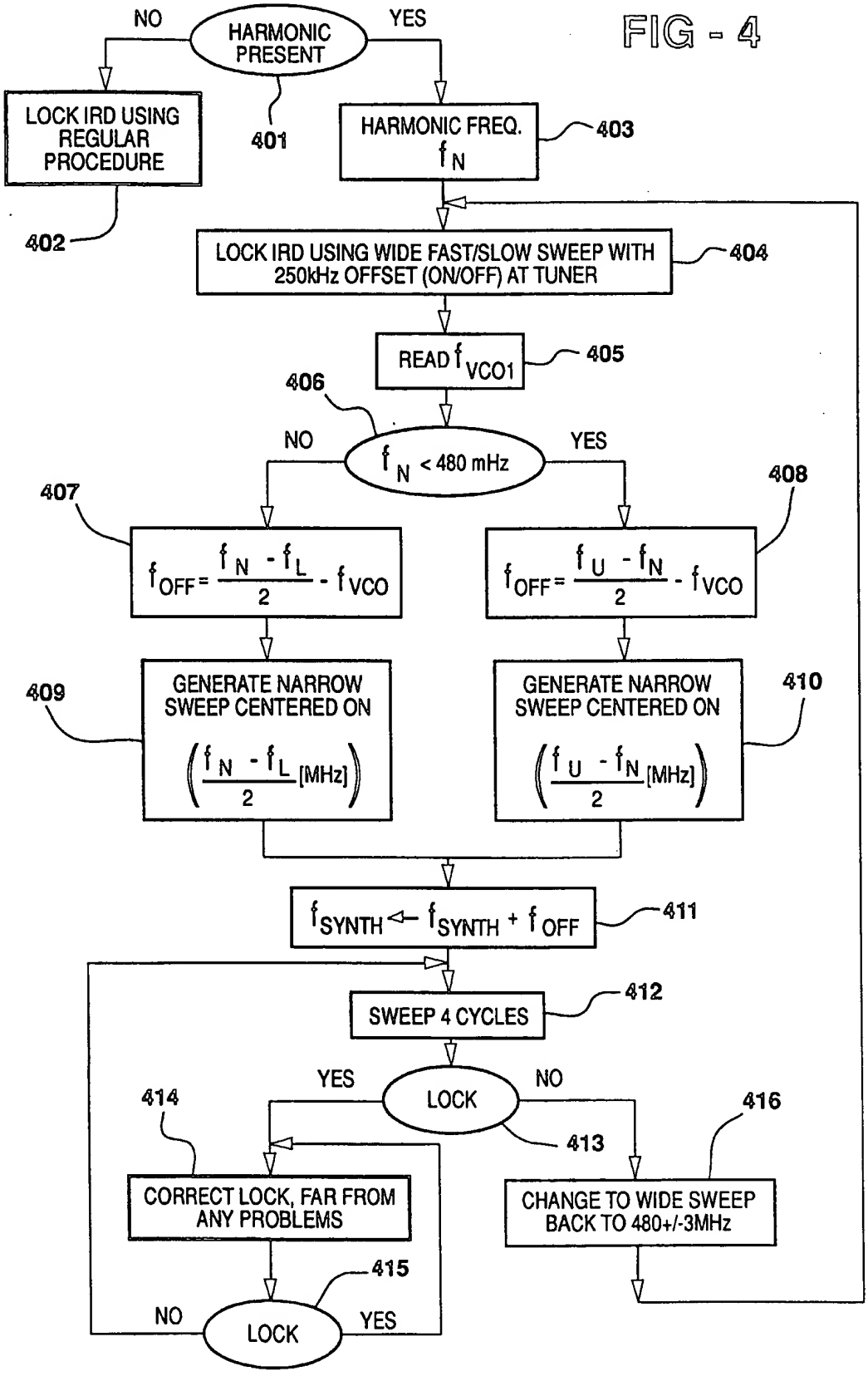
FIG - 4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404
READ f_{VCO1}
405
406
f_N < 480 mHz
NO
YES
407
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$f_{OFF} = \frac{f_U - f_N}{2} - f_{VCO}$
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GENERATE NARROW SWEEP CENTERED ON $\left(\frac{f_N - f_L}{2}\text{[MHz]}\right)$
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LOCK
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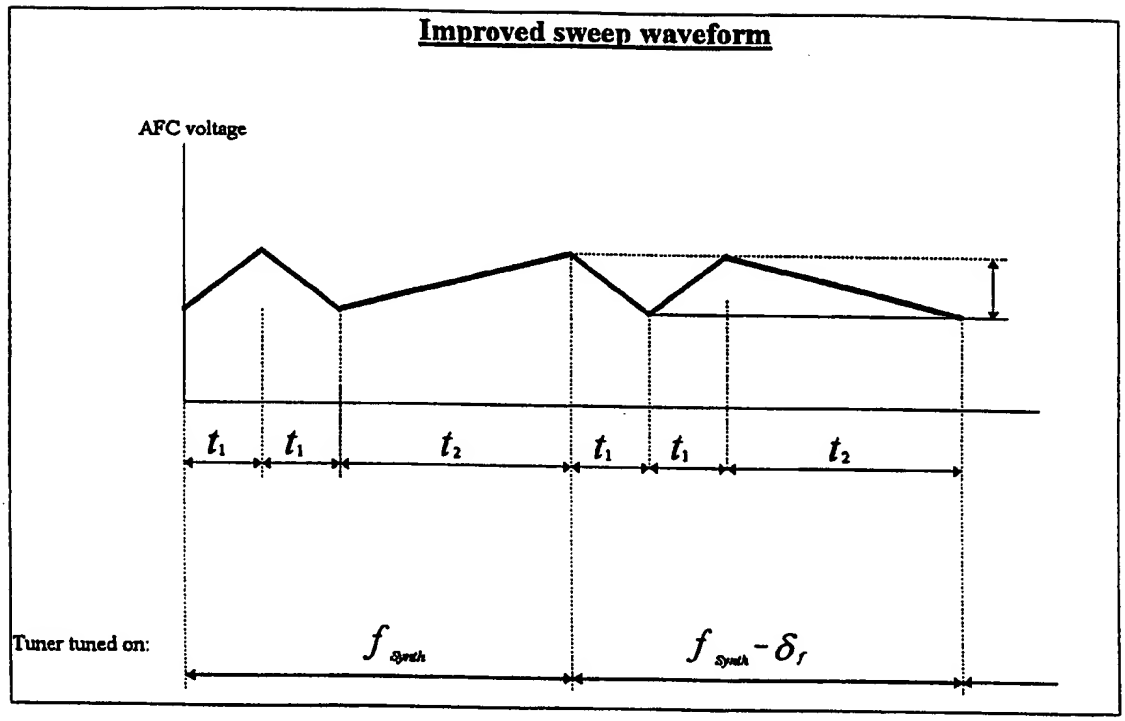
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Figure 6